American University of Beirut  
Faculty of Engineering and Architecture  
Department of Electrical and Computer Engineering

EECE 412L – VLSI Computer Aided Design Lab

Course title: VLSI Computer Aided Design Lab

Course number: EECE 412L

Catalog Description
A VLSI design course that introduces students to the basics of integrated circuits (IC) design using computer aided design (CAD) tools. The lab familiarizes students with the IC design flow using the industry-standard Cadence Design Systems tools. Custom design of basic ICs will be covered at the physical layout, circuit, logic, and system levels. Lab assignments include design and simulation projects using CAD tools for physical layout design, schematic capture, place-and-route of standard cells, logic verification, circuit extraction and simulation.

Credit hours: 1 credit

Required or elective:  
Elective for CCE and ECE students

Prerequisites:
By course: EECE 412 (prerequisite or co-requisite)  
By topic: Digital integrated circuits

Textbook(s) and/or required materials
Lab experiments to be distributed to students in terms of a lab manual.

Course Objectives

<table>
<thead>
<tr>
<th>The objectives of this course are to:</th>
<th>Correlates to program educational objectives</th>
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<tr>
<td>Introduce students to IC CAD design flow using Cadence</td>
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<td>Introduce students to a complete digital IC design cycle: analysis, design, simulation, layout, extraction and verification.</td>
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<td>Develop in students the basic skills needed in VLSI IC design using CAD tools.</td>
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<td>Instill in students the capability of designing and implementing a digital IC block (e.g. ALU) to meet certain design specifications and produce the final physical layout design.</td>
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<td>Foster effective interaction skills and teamwork communication.</td>
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Course Topics and Lab Experiments

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<tr>
<th>No.</th>
<th>Lab Experiments</th>
<th>Sessions</th>
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<tbody>
<tr>
<td>1</td>
<td>HSPICE tutorial: Introduction to HSPICE; netlists (RC filter and inverter); DC, AC and transient analysis</td>
<td>1</td>
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<td>2</td>
<td>Cadence tutorial part 1: Introduction to Cadence environment; setup Linux environment; create schematic and symbol of an inverter</td>
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<td>3</td>
<td>Cadence tutorial part 2: Layout of an inverter, DRC/LVS checks, Extraction and post-layout simulation</td>
<td>2</td>
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<td>4</td>
<td>Design and implementation of complex gates: NOR, NAND and XOR</td>
<td>2</td>
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<tr>
<td>5</td>
<td>Design and Layout of 1-bit full ADDER</td>
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<tr>
<td>6</td>
<td>Design and Layout of 4-bit full ADDER</td>
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Course Learning Outcomes

At the end of the course, students should be able to:

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<th>Correlates to program outcomes*</th>
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<tr>
<td>H</td>
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<tr>
<td>M</td>
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<tr>
<td>L</td>
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Comprehend the design flow for integrated circuit using Cadence.  
Understand the issues related to modern IC manufacturing processes and the various design and testing methodologies.  
Use advanced process technologies to do the physical implementation (Layout) of an IC.  
Use the DRC (Design Rule Check) and LVS (Layout Versus Schematic) for verification.  
Understand the effect of the capacitive and resistive parasitic on the performance of the IC using circuit extraction tools (e.g., Assura RCx).  
Simulate a circuit pre-layout and post-layout using HSPICE.  
Implement a complex hierarchical circuit block based on a given set of performance specifications.

* H: High correlation, M: Medium correlation, L: Low correlation

Lecture schedule
None

Laboratory schedule
One three-hour laboratory session per week

Resources of the course
Reference books, online references, and Moodle.

Computer usage
HSPICE circuit simulator; Cadence design tools: Virtuoso (layout), Assura (DRC, LVS, Rcx), SPECTRE simulator

Evaluation methods
- Participation/Evaluation: 5%
- In-lab experiment work: 40%
- Drop Quizzes: 10%
- Lab reports: 10%
- Project: 35%

Professional component
- Engineering topics: 100%
- Mathematics and basic sciences: 0%
- General education: 0%

Course Policies
- Lab attendance is required
- Students should not miss any lab session except for a valid medical reason
- In case of absence, students should report the case to the instructor in any way (phone, email) directly within the same week of the lab to be missed
- A make-up lab session should be scheduled
• No make-up sessions can be scheduled except within the same week
• Any student who miss any lab session with no make-up will be dropped from the course
• The partner of an absent student from the lab should report to the lab as usual in the normal session time
• Students who are late will not be allowed to attend the lab session and hence are considered absent from the lab session
• Any act of cheating or plagiarism will not be tolerated and will be reported to the disciplinary committee for appropriate disciplinary action.

Person(s) who prepared this description and date of preparation
Mohammad Mansour, Basma Hijazi, May 2012

Date of last revision
May 2012