American University of Beirut
Faculty of Engineering and Architecture
Department of Electrical and Computer Engineering

EECE 634 Optimizing Compilers

Course Syllabus – Spring 2007

Instructor Information

Instructor: Mazen A. R. Saghir
Office: Room 301, Bechtel Engineering Building
Office Hours: Monday and Wednesday: 11:00 am – 1:00 pm; Tuesday: 9:00– 11:00 am
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FEA Mail Box: 59

Course Information

Prerequisites: EECE 330 Data Structures and Algorithms and EECE 421 Computer Architecture; or consent of the instructor.
Lectures: Monday and Wednesday from 3:30 – 4:45 pm.
Room 537, Bechtel Engineering Building
Course Web Site: Moodle


Course Description

This course covers the theoretical and practical aspects of building modern optimizing compilers. Topics include: intermediate representations, basic blocks and flow graphs, data flow analysis, partial evaluation and redundancy elimination, loop optimizations, register allocation, instruction scheduling, and interprocedural analysis. To consolidate the material covered in class, students implement significant optimizations within the framework of a modern research compiler.
Course Objectives

On successfully completing this course, you will be able to:

1. Understand the role of intermediate program representations.
   - Identify the different types of intermediate representations.
   - Explain the main trade-offs between the different types of intermediate representations.
   - Explain how intermediate representations are used to express programs and guide code generation.

2. Understand the principle of control-flow analysis.
   - Use control-flow techniques to identify program structures, such as loops and subroutines, and possible program execution paths.

3. Understand the principle of data-flow analysis.
   - Use data-flow techniques to make various assertions about data usage within a program.
   - Identify appropriate data-flow techniques for applying specific optimizations.

4. Understand the characteristics of common compiler optimizations.
   - Identify the information needed to implement a given optimization.
   - Explain the effects of common optimizations on performance and code size.

5. Understand the characteristics of common loop optimizations.
   - Identify the information needed to implement various loop optimizations.
   - Explain the effects of various loop optimizations on performance and code size.

   - Explain how variables or intermediate results are allocated to machine registers.
   - Explain the trade-offs between storing variables in machine registers and main memory.

7. Understand instruction scheduling techniques.
   - Explain the relationship between instruction scheduling and execution performance.
   - Generate an appropriate code schedule for a given instruction-set architecture.
   - Identify opportunities for exploiting instruction-level parallelism.

8. Understand how compilers exploit parallelism to enhance execution performance.
   - Identify opportunities for exploiting fine-grained parallelism.
   - Identify opportunities for exploiting coarse-grained parallelism.

Grading

- Project 40%
- Midterm Exam 25%
- Final Exam 35%
**Tentative Course Schedule**

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**Exam Schedule**

Midterm Exam       Saturday, March 24th, 2007 at 9:00 am in Wing D.
Final Exam         TBD by the Registrar’s Office.